

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached page is captioned "Version With Markings To Show Changes Made."

REJECTIONS UNDER 35 U.S.C. §102 AND 103

Claims 1, 2, 7, 8, 13, 18 and 19 were rejected under 35 U.S.C. §102(e) as allegedly being anticipated by Przydatek et al. (U.S. '155, hereinafter "Przydatek"). Applicant respectfully traverses this rejection.

For a reference to anticipate a claim, each element must be disclosed, either expressly or under principles of inherency, by the reference. Applicant respectfully submits that Przydatek fails to disclose each element of the claimed invention. For example, Applicant submits that Przydatek fails to disclose a plurality of switching circuits, each circuit coupled to a respective transformer and further adapted to switch to multiple positions depending on whether the current flowing through a primary circuit of a respective transformer is in a metering range or an overcurrent range, as required by claim 2 and its dependents. Similar comments apply to independent claim 13 and its dependents. Applicant also submits that Przydatek fails to disclose causing switching circuits to switch to multiple positions depending on whether current flowing through a primary circuit of a respective transformer is in a metering range or an overcurrent range, as required by independent claims 7 and 18 and their respective dependents.

The above claimed feature is supported by, for example, the exemplary embodiment illustrated in Figure 2 of the application. Figure 2 shows a switching

integrated circuit (SIC) U2 connected to a winding of a transformer T1. When field current flowing through a primary winding of transformer T1 is in a metering range, pins 10 and 11 and pins 14 and 15 of SIC U2 engages resistance 38, thereby developing a voltage at pin 10. The voltage developed at pin 10 is proportional to the current flowing in the primary winding of transformer T1. When the field current flowing through the primary winding of transformer T1 is in an overcurrent (DFR) range, resistance 39 is engaged by closing contacts at pins 2 and 3 and pins 6 and 7, and opening contacts at pins 14 and 15 and pins 10 and 11, thereby developing a voltage at pin 7. The voltage developed at pin 7 is proportional to the current flowing in the primary winding of transformer T1. The contacts at pins 2 and 3, pins 6 and 7, pins 10 and 11, and pins 14 and 15 may therefore be switched depending on whether current flowing through a primary circuit of a respective transformer is in a metering range or an overcurrent range.

Przydatek fails to disclose the above claimed features. For example, Przydatek explicitly teaches the following (*emphasis added*) on Col. 7, lines 31-39:

Referring also to FIG. 1, the transducers 16 **permanently connect, i.e., without mechanical switching**, each gain channel signal to at least one ADC 18. The ADC samples the analog current and voltage in each phase for each gain channel of the electric circuit 14, and converts the analog signal to a digital signal for each gain channel. Thus, information is gathered for all gain channel signals **at all times**, even if the gain channel signal is saturated, to guarantee no missing or clipped samples.

The Office Action apparently alleges that voltage transducers and amplifiers 16 of Przydatek disclose the above claimed features. (See section 2 of the Office Action).

Applicant respectfully disagrees. Col. 7, lines 31-39 of Przydatek explicitly discloses that transducers 16 permanently connect each gain channel signal to at least one ADC 18 without switching. The information for all gain channel signals is therefore gathered at all times. Przydatek therefore teaches away from a plurality of switching circuits coupled to respective transformers and adapted to switch to multiple positions depending on whether the current flowing through a primary circuit of a respective transformers is in a metering range or an overcurrent range.

The Office Action apparently further alleges that the above claimed features are disclosed by Col. 4, lines 20-39. (See last line of section 2 of the Office Action).

Applicant again respectfully disagrees. Col. 4, lines 20-39 discloses a processor which selects from among alternate gain channels. As illustrated in Figures 2 and 5-6 and as discussed, for example, on col. 8, line 58 to col. 9, line 13, digital signal processor (DSP) 20 executes a gain control algorithm that may reside in flash memory of CPU 22. In the gain control algorithm, DSP 20 scans all gain channels, sample by sample, to eliminate saturated channels, and selects optimal gain channels. Gain selection information is stored in an internal data structure on DSP 20. While Przydatek discloses digital signal processor 20 selecting between alternate gain channels, Przydatek fails to disclose switching circuits (an element which is distinct from the digital signal processor) switching between multiple positions, let alone switching circuits coupled to respective transformers for switching between multiple positions depending on whether the current flowing through a primary circuit of a respective transformer is in a metering range or an

overcurrent range. Digital signal processor 20 of Przydatek, which merely selects between alternate gain channels, does not disclose a switching circuit, let alone a switching circuit coupled to a transformer which switches between multiple positions.

Accordingly, Applicant submits that still pending claims 2, 7, 8, 13, 18 and 19 are not anticipated by Przydatek, and respectfully requests that the rejection of these claims under 35 U.S.C. §102(e) be withdrawn.

Claims 3, 4, 5, 9, 10, 14, 15, 17, 20 and 21 were rejected under 35 U.S.C. §103 as allegedly being unpatentable over Przydatek in view of Lusignan et al. (U.S. '209, hereinafter "Lusignan"). Claims 6, 11, 12, 16 and 22 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Przydatek in view of Lusignan and further in view of Farrington et al. (U.S. '451, hereinafter "Farrington"). Applicant respectfully traverses these rejections. Since each of these claims depends from one of independent claims 1, 7, 13 or 18, Applicant submits that the above comments regarding Przydatek apply equally to these claims. Applicant submits that neither Lusignan and/or Farrington remedies the above deficiencies of Przydatek. Applicant therefore respectfully submits that the above rejections under 35 U.S.C. §103 be withdrawn.

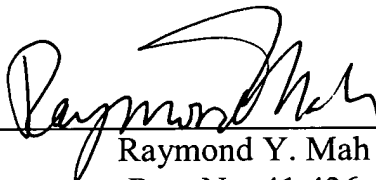
GAMVRELIS et al
Serial No. **09/878,920**
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CONCLUSION

Applicant respectfully submits that this application is in condition for allowance and respectfully requests a Notice to this effect. If the Examiner has any questions or believes that an interview will further prosecution of this application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

2. (Amended) A multifunction apparatus for monitoring and reporting electric signals on electric circuits, comprising:

a first system for receiving input data from at least a field transformer or a line post sensor;

a digital signal processor (DSP) system coupled to said first system;

a microprocessor system coupled to said DSP system; and

said first system in combination with said DSP system and said microprocessor system perform metering, power quality, digital fault recording (DFR) and supervisory control and data acquisition (SCADA) functions[.]; [The apparatus of claim 1]

wherein said first system comprises:

a plurality of transformers, each transformer operating with respect to one phase of an electric circuit; and

a plurality of switching circuits, each circuit coupled to a respective transformer and further adapted to switch to multiple positions depending on whether the current flowing through a primary circuit of a respective transformer is in a metering range or an overcurrent range.